WHAT IS CLAIMED IS:

1. An integrated circuit incorporating an Electrostatic Discharge (ESD) protection device comprising:

a semiconductor substrate;

an electrical contact pad;

an ESD switch coupled to the pad and having an active device region formed in the semiconductor substrate; and

a dynamic shock absorbing region formed in the semiconductor substrate adjacent to said active device region, said dynamic shock absorbing region made from a material with thermo-mechanical properties substantially more resistant to shock from dynamic effects of ESD than said active device region.

2. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said thermo-mechanical properties include a dynamic loss factor higher than approximately 0.01.

3. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said thermo-mechanical properties further include a melting temperature higher than approximately 800 °K.

4. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said thermo-mechanical properties further include a moderately low stiffness as defined by an elastic modulus approximately in the range of 10 GPa and 100 GPa (Giga Pascals).

5. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said thermo-mechanical properties further include a tensile strength higher than approximately 100 MPa.

6. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein the ESD switch has one or more sides, and wherein the dynamic shock absorbing region formed in the semiconductor substrate is located in trenches adjacent to the one or more sides of the ESD switch.

7. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein the ESD switch is a transistor.

8. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein the dynamic shock absorbing region is configured above the active device region.

9. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein the dynamic shock absorbing region is configured below the active device region of the ESD switch.

10. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said dynamic shock absorbing region made from a material with thermo-mechanical properties substantially more resistant to dynamic shock than said active device region is selected from the group consisting of hard polymers, amorphous carbon, carbon-carbon composite or carbon-polymer composite.

11. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 1, wherein said dynamic shock absorbing region is surrounded by a dielectric region.

12. An integrated circuit incorporating an Electrostatic Discharge (ESD) protection device comprising:

a semiconductor substrate;

an ESD switch having an active device region formed in the semiconductor substrate; and

a plurality of dynamic shock absorbing regions formed around the active device region, said dynamic shock absorbing region made from a material with thermo-mechanical properties substantially more resistant to shock from dynamic effects of ESD than said active device region.

13. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein said thermo-mechanical properties include a dynamic loss factor higher than approximately 0.01.

14. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein said thermo-mechanical properties further include a melting temperature higher than approximately 800 °K.

15. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein said thermo-mechanical properties further include a moderately low stiffness as defined by an elastic modulus approximately in the range of 10 GPa and 100 GPa (Giga Pascals).

16. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein said thermo-mechanical properties further include a moderately high tensile strength higher than approximately 100 MPa.

17. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, further comprising a dielectric layer formed in between said ESD switch and said dynamic shock absorbing region.

18. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12 and further comprising a passivation layer formed above said dynamic shock absorbing region.

19. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein said ESD switch has a gate region and wherein said gate region is formed from a thermo-mechanical energy sink material, said thermo-mechanical energy sink material substantially more resistant to thermo-mechanical expansion than the semiconductor substrate.

20. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 19, wherein said thermo-mechanical energy sink material has physical properties including a high melting temperature higher than approximately 2000 °K.

21. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 19, wherein said thermo-mechanical energy sink material has physical properties further including a high tensile strength higher than approximately 300 MPa.

22. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 19, wherein said thermo-mechanical energy sink material has physical properties further including a low thermal expansion coefficient lower than approximately 5×10^{-6} $°K^{-1}$.

23. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, further comprising a second dynamic shock absorbing region formed in the semiconductor substrate in thermal contact with said active device region, said second dynamic shock absorbing region made from a material with thermo-mechanical properties substantially more resistant to shock from the dynamic effects of ESD than said active device region.

24. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 12, wherein the ESD switch has one or more sides, the device further comprising a third dynamic shock absorbing region located adjacent to the one or more sides of the ESD switch.

25. An integrated circuit incorporating an Electrostatic Discharge (ESD) protection device comprising:

a semiconductor substrate;

an ESD circuit comprising a switch having an active device region formed in the semiconductor substrate and one or more passive circuit components; and

means for absorbing dynamic shock from at least one of the switch and one or more passive components in response to an ESD event.

26. An integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 25, wherein said means for absorbing shock comprises a region above the active device region made from a material with thermo-mechanical properties resistant to shock from

dynamic effects of ESD, the thermo-mechanical properties including a high material dynamic loss factor higher than approximately 0.01.

27. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 25, and further comprising a second dynamic shock absorbing region formed below the active device region, said second dynamic shock absorbing region made from a material with thermo-mechanical properties resistant to shock from the dynamic effects of ESD, the thermo-mechanical properties including a high material dynamic loss factor higher than approximately 0.01.

28. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 25, wherein the ESD switch also has one or more sides, wherein the means for absorbing shock further comprises a third dynamic shock absorbing region formed adjacent to the one or more sides of the ESD switch, said third dynamic shock absorbing region made from a material with thermo-mechanical properties resistant to shock from the dynamic effects of ESD, the thermo-mechanical properties including a high material dynamic loss factor higher than approximately 0.01.

29. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 25, wherein said ESD switch has a gate region and wherein said gate region is formed from a thermo-mechanical energy sink material, said thermo-mechanical energy sink material substantially resistant to thermo-mechanical expansion and having physical properties including a low thermal expansion coefficient lower than approximately 5×10^{-6} $°K^{-1}$.

30. The integrated circuit incorporating an Electrostatic Discharge (ESD) protection device according to claim 25, wherein said active device region is formed from a thermo-mechanical energy sink material, said thermo-mechanical energy sink material substantially resistant to thermo-mechanical

expansion and having physical properties including a low thermal expansion coefficient lower than approximately 5×10^{-6} °K^{-1}.

31. A method of fabricating an ESD device on a semiconductor substrate, the method comprising:

fabricating a switch from connectors and active device regions formed in the semiconductor substrate;

providing a dynamic shock absorbing region formed in the semiconductor substrate adjacent said active device regions, said dynamic shock absorbing region made from a material with thermo-mechanical properties substantially resistant to shock from dynamic effects of ESD.

32. A method of fabricating an ESD device on a semiconductor substrate according to claim 31, wherein said thermo-mechanical properties including a high material dynamic loss factor higher than approximately 0.01.

33. The method of fabricating an ESD device on a semiconductor substrate according to claim 31 wherein said thermo-mechanical properties further include a moderate melting temperature material higher than approximately 800 °K.

34. The method of fabricating an ESD device on a semiconductor substrate according to claim 31, wherein said thermo-mechanical properties further include a moderately low stiffness as defined by an elastic modulus approximately in the range of 10 GPa to 100 GPa (Giga Pascals).

35. The method of fabricating an ESD device on a semiconductor substrate according to claim 31, wherein said thermo-mechanical properties further include a moderately high tensile strength higher than approximately 100 MPa.